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1. (Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

(a) field oxide layer disposed on a semiconductor substrate;

(b) a metal plug contact disposed within a contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer; and

(c) a metal connected to said metal plug contact.

2. The device as claimed in claim 1, wherein said semiconducting device comprises integrated circuits.

3. The device as claimed in claim 1, wherein said field oxide layer further comprises silicon oxide.

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4. The device as claimed in claim 2, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

5. (Amended) A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) providing a field oxide layer disposed on a semiconductor substrate;

(b) providing a metal plug contact disposed within a contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer; and

(c) connecting a metal to said metal plug contact.

6. The method as claimed in claim 5, wherein said semiconducting device comprises integrated circuits.

7. The method as claimed in claim 5, wherein said field oxide layer further comprises silicon

oxide.

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8. The method as claimed in claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

9. (Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

(a) field oxide layer disposed on a semiconductor substrate;

(b) a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is isolated from said contact region; and

(c) a metal connected to said metal plug contact.

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10. The device as claimed in claim 9, wherein said semiconducting device comprises integrated circuits.

11. The device as claimed in claim 9, wherein said field oxide layer further comprises silicon oxide.

12. The device as claimed in claim 10, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

13. (Amended) A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) providing a field oxide layer disposed on a semiconductor substrate;

(b) providing a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is isolated from said contact region; and

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(c) connecting a metal to said metal plug contact.

14. The method as claimed in claim 13, wherein said semiconducting device comprises integrated circuits.

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15. The method as claimed in claim 13, wherein said field oxide layer further comprises silicon oxide.

16. The method as claimed in claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

17. The device as claimed in claim 1, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

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18. The method as claimed in claim 5, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

19. The device as claimed in claim 9, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

20. The method as claimed in claim 13, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

23. The device of claim 9, wherein said metal plug contact contacts said field oxide layer.

24. The method of claim 13, wherein said metal plug contact contacts said field oxide layer.